IN THE SPECIFICATION

Please amend the paragraph at page 1, lines 14-20 as follows:

A top view of a conventional NOR type non volatile semiconductor memory device is shown in Fig. 8 [[6]]. As shown in Fig. 8 [[6]], a plurality of element region (ER)are arranged in a horizontal direction of the Fig. 8 [6]. Each of the element regions is electrically separated from each other by element isolation regions STI (Shallow Trench Isolation). A plurality of word lines WL1 portions of which are used as gate electrodes are arranged in a vertical direction of Fig. 8 [[6]] so as to intersect each of the element regions.

Please amend the paragraph at page 2, lines 1-5 as follows:

Figs. 6 [[4]] and 7 [5]] show cross sectional views of the A-A and the B-B shown in Fig. 8 [[6]] respectively. As shown in Fig. 8 [[5]], a plurality of element isolation regions (STI) are formed on an upper surface of the semiconductor substrate 100, thereby forming a plurality of element regions each of which is arranged between the two element isolation regions. A word line WL1 is formed so as to intersect each of the element regions.

Please amend the paragraph at page 2, lines 6-12 as follows:

As shown in Figs. 6 and 8 ~~4 and 5~~, the word line WL1 is formed on a silicon oxide layer 101 (a first gate insulating film) that is formed on the semiconductor substrate 100. The word line WL1 also includes a poly crystalline silicon layer 104 that is used as a first floating gate, a poly crystalline silicon layer 105 that is used as a second floating gate, an ONO layer 106 that is used as a second gate insulating film, a

control gate electrode comprised of a poly crystalline silicon layer 107 and a tungsten silicide ~~silicon~~ layer 108 (WSi), and a TEOS layer 109 that was used as a mask layer to form a gate electrode.

Please amend the paragraph at page 2, lines 21-27 as follows:

Portions of a silicon oxide layer 101, a silicon nitride layer 111, silicon oxide layers 112 and 131 are removed to a direction vertical to the element region and the element isolation region, and parallel to the word line WL1 by using a RIE method (Reactive Ion Etching), thereby forming a contact hole to reach source regions that are formed on an upper surface of the semiconductor substrate 100. And then [[the]], a metal layer 114b , for instance, tungsten layer W is formed in the contact hole, thereby forming a source line 103.

Please amend the paragraph at page 2, line 28 through page 3, line 2 as follows:

After that, a silicon oxide layer 113 that is used as an interlayer insulating layer is formed and flatted by using a CMP (Chemical Mechanical Polishing) method. At positions where the source line 103 is not formed, portions of a silicon oxide layer 101, a silicon nitride layer 111, silicon oxide layers 112, 131, and 113 are removed so as to expose upper surfaces of the silicon substrate 100 by using a RIE method, thereby forming contact holes. A metal layer 114a, for instance, tungsten W is then formed in the contact hole, thereby forming drain contacts 102a. After that, a portion of the silicon oxide layer 112 is removed so as to expose an upper surface of the source line 103 by using a RIE method, thereby forming a contact hole. A metal layer 116, for instance, tungsten W is then formed in the contact hole, thereby

forming a source contact 102b that electrically connects between the source line 103 and line layer (not shown).

Please amend the paragraph at page 3, lines 3-7 as follows:

It is noted that [[a]] conventional semiconductor memory devices with [[a]] source line structures [structure] are shown in following materials. IEDM98-975-978 (Novel 0.44 μm2 Ti-Salicide STI Cell Technology for High-Density NOR Flash Memories and High Performance Embedded Application), Japanese patent laid open Hei10-326896, Hei6-334156, Hei7-74325, Hei11-265947, 2002-76147, Hei9-129854, and 2001-68571.

Please amend the paragraph at page 3, lines 21-29 as follows:

A first aspect of the present invention is providing a semiconductor memory device having a gate electrode and a diffusion layer, comprising a plurality of memory cells each of which including the gate electrode and the diffusion layers; a first contact layer connected to one of the diffusion layer of the memory cell; a second contact layer connected to the first contact layer; a bit line connected to the second contact layer; and a conductive layer connected to at least two of the diffusion layers that are other than the diffusion layer connected to the first contact layer, at least two of the diffusion layers being arranged in a direction vertical to the bit line, a height of the conductive layer substantially being the same as a height of the first contact layer.

Please amend the paragraph at page 3, line 30, through page 4, line 8, as follows:

A second aspect of the present invention is providing a semiconductor memory device having a gate electrode and a diffusion layer, comprising a plurality of memory cells each of

which including the gate electrode and the diffusion layer; an insulating film formed above side and top surfaces of the gate electrode of the semiconductor memory device; a first interlayer insulating layer formed between the gate electrode of the semiconductor memory device; a first contact layer formed in the first interlayer insulating layer and connected to the diffusion layer; a second interlayer insulting layer formed on the first inter layer insulating layer ; a second contact layer formed in the second interlayer insulating layer and connected to the first contact layer; a bit line connected to the second contact layer; and a conductive layer connected to at least two of the diffusion layers that are other than the diffusion layer connected to the first contact layer, at least two of the diffusion layers being arranged in a direction vertical to the bit line, a height of the conductive layer substantially being the same as a height of the first contact layer.

Please amend the paragraph at page 6, lines 22-28 as follows:

As shown in Figs. 1 and 2, the word line WL2 is formed on a silicon oxide layer 201 (a first gate insulating film) that is formed on the semiconductor substrate 200. The word line WL2 also includes a poly crystalline silicon layer 204 that is used as a first floating gate, a poly crystalline silicon layer 205 that is used as a second floating gate, an ONO layer 206 that is used as a second gate insulating film, a control gate electrode comprised of a poly crystalline silicon layer 207 and a tungsten silicide [silicon] layer 208 (WSi), and a TEOS layer 209 that was used as a mask layer to form a gate electrode.

Please amend the paragraph at page 7, lines 3-8 as follows:

Portions of the silicon oxide layer 201 and the silicon substrate 200 are removed by using a RIE method and the patterned poly crystalline silicon layer 204 as a mask, thereby

forming trench grooves of STI (Shallow Trench Isolation) in an upper surface of the silicon substrate 200. After that, a silicon oxide layer (not shown) is formed on the upper surface of the silicon substrate 200 and an [[a]] inner wall of the trench grooves of the STI by using a thermal oxide method.

Please amend the paragraph at page 8, lines 7-10 as follows:

It is noted that the silicon oxide layer 231 may be flattened by using a CMP method so as to expose the upper surface of the silicon nitride layer 211 that is formed above the gate electrode. In this case, a height of the silicon oxide layer 231 can be lowered. In this result, we can get a [[gat]] low etching ratio.

Please amend the paragraph at page 8, line 34, through page 9, line 4 as follows:

From this embodiment of the present invention, the same photo mask can be used at the manufacturing step of the drain contact 202a and the source line 203. Moreover, the same mask can be used at the manufacturing step of the contact holes 219 and 216. Therefore, a height of the drain contact 202a is the same as that of the source line 203, and a height of the contact hole 219 is the same as that of the contact hole 216. From this, the aspect ratio of the drain contact 202a can be made lower, thereby resulting in preventing a poor conduction.

Please amend the paragraph at page 9, lines 5-10 as follows:

As stated above, in the conventional technique, a photo mask by which the drain contact is formed is different from a photo mask by which the source line. On the other hand, in this embodiment of the present invention, the photo mask by which the drain contact 202a is formed is the same as photo mask by which the source line 203 is formed. Therefore, it can

enhance a precision of patterning, resulting in preventing a poor conduction as even downsizing progressed.